

S1R72U01

Data Sheet

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1. Overview

The S1R72U01 is a serial (UART) - USB 2.0 host/device bridge LSI supporting USB 2.0 FS/LS. The main CPU controls the LSI's USB functions using simplified commands. No USB driver is required. The USB class supported is the Human Interface Device class.

2. Features

2. Features

■ Ease of use and easy connections (serial connections)

Uses simplified commands to control USB functions

The main CPU controls this LSI's USB functions using simplified commands. No USB driver needs to be installed.

The UART (2-wire asynchronous) serial interface permits the easy connection of various CPU types.

■ Built-in regulator

USB regulator

Core voltage regulator

The S1R72U01 has two regulators: one (input range: 3.3 to 5.0 V) to generate 3.3 V for the USB and another (input voltage: 3.3 to 5.0 V) to generate the internal core voltage of 1.8 V. This allows the S1R72U01 to operate from a single power source as long as the supplied voltage is at least 3.3 V.

■ Built-in VBUS supply function

No external VBUS power SW required

The S1R72U01 features a built-in VBUS supply function for USB host operations, eliminating the need for the external VBUS power SW previously required by the USB host controller. The S1R72U01 features an interface that controls the external VBUS power SW if the built-in VBUS supply function cannot supply adequate current. If necessary, connect an external VBUS power SW to ensure sufficient current capacity for bus-powered devices.

■ Product (system) development support function

History display

The S1R72U01 uses a serial interface (asynchronous type) to display the history of internal LSI processing, etc. This function provides useful information during product (system) development.

3. Block Diagram

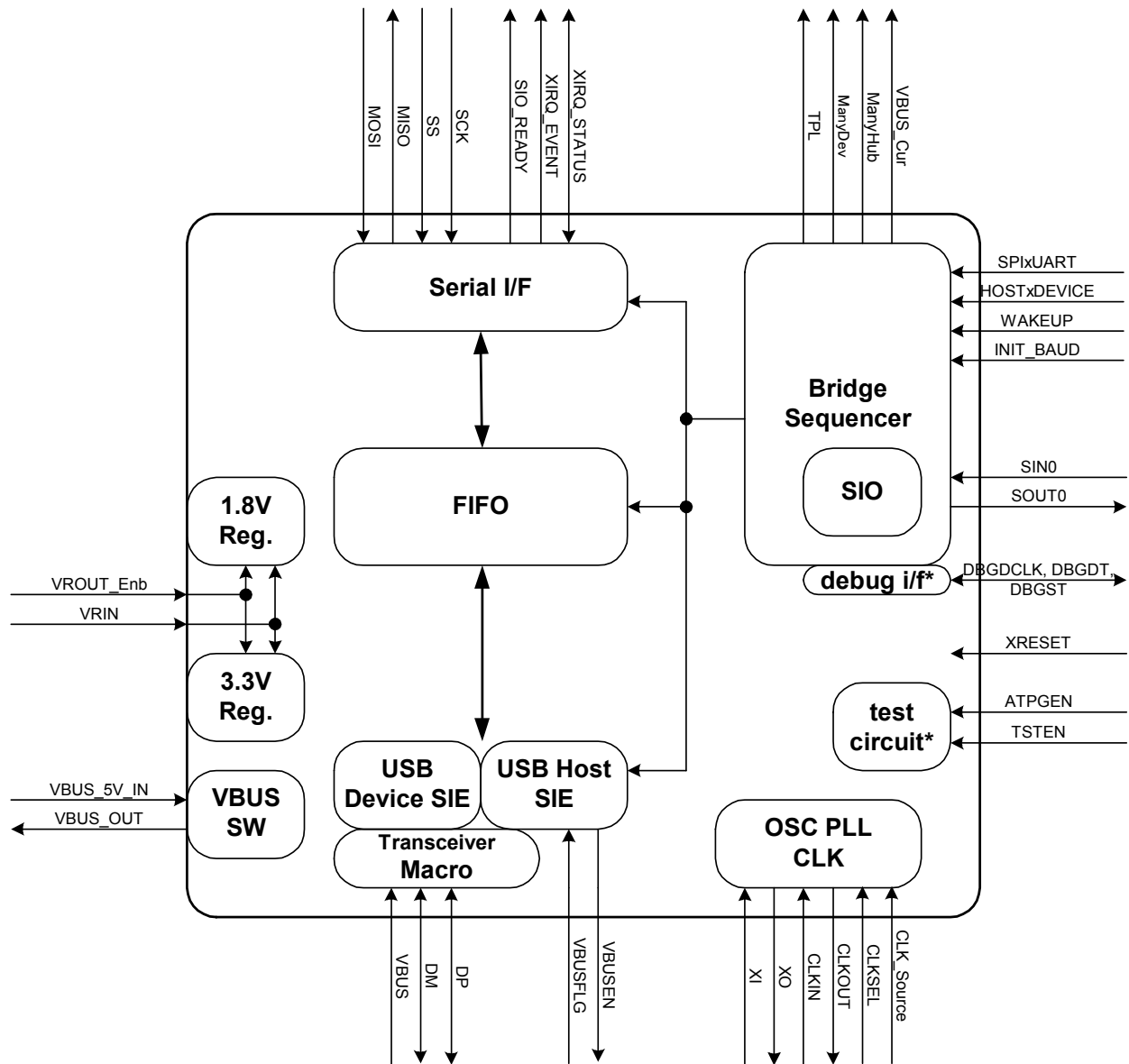


Fig. 3-1 Block diagram

4. Functions

4. Functions

4.1 Serial I/F (UART)

The S1R72U01 is connected to the main CPU via UART (2-wire asynchronous system). Set the SPIxUART mode setting pin to Low.

The interface voltage (CVDD) can be used across a broad range, from 1.8 to 5.0 V.

- UART connection (asynchronous serial I/F)

Initial baud rate: 300/9600 bps (set by mode setting pin INIT_BAUD)

Baud rate: Settable (max. 3 Mbps)

LSb first

8-bit data

1/2 stop bit

Odd/Even/No parity

4.2 USB Host SIE

The USB host function complies with the USB 2.0 (Universal Serial Bus Specification Revision 2.0) standard. It supports FS (12 Mbps) and LS (1.5 Mbps) speed modes. The USB functions are controlled by the Bridge Sequencer block inside the LSI. The USB class supported is the Human Interface Device Class.

4.3 USB Device SIE

The USB device function complies with the USB 2.0 (Universal Serial Bus Specification Revision 2.0) standard. It supports FS (12 Mbps) speed mode. The USB function is controlled by the Bridge Sequencer block inside the LSI. The USB class supported is the Human Interface Device Class.

4.4 Transceiver Macro

This is a USB analog macro block shared by host and device.

4.5 FIFO

This FIFO block serves as a buffer for data between the serial interface and the USB.

4.6 Bridge Sequencer

This controls the USB functions based on commands from the serial interface.

4.7 SIO

This block is used to display the history of the product (system) development support functions and for analog tests.

4.8 Debug I/F

This is a debugging pin for the built-in Bridge Sequencer. It is not intended for use by the user and should be disregarded.

4.9 1.8-V Regulator

This regulator generates 1.8-V internal core voltage. The range of input voltages is from 3.3 to 5.0 V.

4.10 3.3-V Regulator

This regulator generates 3.3 V for the USB. The range of input voltages is from 3.3 to 5.0 V.

4.11 VBUS SW

This is a VBUS output block built into the LSI.

4.12 Test Circuit

This is a circuit for IC tests. It is not intended for use by the user and should be disregarded.

6. Pin Functions

GENERAL (CVDD system)					
BGA	QFP	Name	I/O	RESET	Pin description
-	29	XRESET	IN	-	Reset signal
-	39	CLKSEL	IN	-	Clock frequency selection 1: 24 MHz 0: 12 MHz
-	41	CLK_Source	IN	-	Clock source selection 1: CLKIN 0: XI
-	40	CLKIN	IN	-	Clock input 12 MHz / 24MHz
-	42	CLKOUT	OUT	Low	Clock output Refer to the S1R72U01 Technical Manual for information on how to change the clock output. 48 MHz / 24 MHz / 12 MHz / 6 MHz / 3 MHz / STOP

OSC (LVDD system)					
BGA	QFP	Name	I/O	RESET	Pin description
-	10	XI	IN	-	Internal oscillator circuit input 12 MHz / 24 MHz
-	11	XO	OUT	-	Internal oscillator circuit output

TEST (LVDD, CVDD systems)					
BGA	QFP	Name	I/O	RESET	Pin description
-	44	TSTEN	IN(PD)	-	Test pin (*1); not intended for use by user
-	37	ATPGEN	IN(PD)	-	Test pin (*1); not intended for use by user

PD: Pull-down I/Os are used.

*1: This is pulled down inside the LSI. However, we recommend fixing it at Low on the circuit board.

USB (UVDD3 system)					
BGA	QFP	Name	I/O	RESET	Pin description
-	9	VBUS	IN	-	VBUS input pin
-	8	DP	BI	Hi-Z	USB data line Data+
-	7	DM	BI	Hi-Z	USB data line Data-

PU: Pull-up I/Os are used.

VBUS (UVDD3 system)					
BGA	QFP	Name	I/O	RESET	Pin description
-	12	VBUSFLG	IN(PU)	-	USB power switch fault detection signal 1: Normal, 0: Error CMOS Schmitt input
-	13	VBUSEN	OUT	Low	USB power switch control signal

6. Pin Functions

Serial I/F (CVDD system): Main CPU

BGA	QFP	Name	I/O	RESET	Pin description
-	30	MISO	Tri	High	Serial data output (Hi-z is output when the SS pin is set to High.)
-	28	MOSI	IN	-	Serial data input
-	31	SS	IN	-	Slave selection (Can be used to control output from the MISO pin. If Hi-z output is not required, fix this pin at Low.)
-	33	SCK	IN	-	Serial clock (not used: fix at Low)
-	25	SIO_READY	OUT	Low	Communication ready notification pin
-	27	XIRQ_STATUS	OUT	High	Status notification
-	26	XIRQ_EVENT	OUT	High	Event read request

Serial I/F (UVDD3 system): History Display

BGA	QFP	Name	I/O	RESET	Pin description
-	15	SIN0	IN(PU)	-	Asynchronous serial data IN
-	14	SOUT0	OUT	High	Asynchronous serial data OUT

PU: Pull-up I/Os are used.

DEBUG I/F (UVDD3 system)

BGA	QFP	Name	I/O	RESET	Pin description
-	16	DBGDCLK	OUT	High	Not used (*1)
-	18	DBGDT	BI(PU)	-	Not used (*2)
-	17	DBGST	OUT	Low	Not used (*1)

PU: Pull-up I/Os are used.

*1: Leave open.

*2: This is pulled up in the LSI. However, an external pull-up of about 10 k Ω is recommended.

GPI (CVDD system)

BGA	QFP	Name	I/O	RESET	Pin description
-	34	SPIxUART	IN	-	Setting pin (fix at Low) 0: UART mode
-	35	HOSTxDEVICE	IN	-	Setting pin 1: HOST mode, 0: DEVICE mode Switching modes resets the LSI.
-	36	WAKEUP	IN	-	Wake-up pin Rising edge activates the wake-up trigger.
-	38	INIT_BAUD	IN	-	Setting terminal 1: 9600bps 0: 300bps

6. Pin Functions

GPO (CVDD system)

BGA	QFP	Name	I/O	RESET	Pin description
-	24	TPL	OUT	Low	Unsupported Device 1: Error, 0: -
-	23	ManyDev	OUT	Low	Too Many Devices 1: Error, 0: -
-	22	ManyHub	OUT	Low	Too Many Hubs 1: Error, 0: -
-	21	VBUS_Cur	OUT	Low	VBUS Over Current 1: Error, 0: -

Regulator (VRIN system)

BGA	QFP	Name	I/O	RESET	Pin description
-	4, 47	VRIN	Power	-	Regulator input (3.3 to 5.0 V) Connect Cin = 1.0 μ F to each pin. Keep this open when not using the regulator.
-	45	VROUT_Enb	IN	-	Enables the regulator Set this to the same level as VRIN when using the regulator. Set this to Low when not using the regulator.

VBUS SW (VBUS_5V_IN system)

BGA	QFP	Name	I/O	RESET	Pin description
-	2	VBUS_5V_IN	Power	-	VBUS generation input (5.0 V)
-	1	VBUS_OUT	Power	-	VBUS output

POWER

BGA	QFP	Name	Voltage	Pin description
-	5	UVDD3	3.3V	Power supply for USB When using regulator: Connect Cout = 1.0 μ F. When not using regulator: Apply the voltage indicated to the left.
-	46	LVDD	1.8V	Internal power supply, test power supply, OSC power supply When using regulator: Connect Cout = 1.0 μ F. When not using regulator: Apply the voltage indicated to the left.
-	32	CVDD	1.8 to 5.0V	Power supply for main CPU I/F
-	3, 6, 20, 43, 48	VSS	0V	GND

7. Commands

7. Commands

7.1 Commands

Communication with the main CPU is implemented via commands. For detailed information on commands, refer to the *S1R72U01 Technical Manual*.

8. Electrical Characteristics

8.1 Absolute Maximum Ratings

Item	Code	Rating	Unit
Power supply voltage	UVDD3 CVDD VRIN VBUS_5V_IN	-0.3 to 7.0	V
	LVDD	-0.3 to 2.5	V
Input voltage	VI	-0.3 to $^{*}+0.5$	V
Output voltage	VO	-0.3 to $^{*}+0.5$	V
Output current/pin	Iout	± 10	mA
Storage temperature	Tstg	-65 to 150	$^{\circ}\text{C}$

* Check the applied voltage of each power supply.

8.2 Recommended Operating Conditions

Item	Code	Min.	Typ.	Max.	Unit
Power supply voltage	UVDD3	3.00	3.30	3.60	V
	CVDD	1.65	1.80 to 5.00	5.50	V
	VRIN		3.30 to 5.00		V
	VBUS_5V_IN		5.00		V
	LVDD	1.65	1.80	1.95	V
Input voltage (*2)	HVI	-0.3	-	HVDD+0.3	V
	LVI	-0.3	-	LVDD+0.3	V
Ambient temperature	T _a	-40	25	85	$^{\circ}\text{C}$

[Precautions for power ON sequence]

Note the following when supplying power from an external source without using the built-in regulator.

Confirm LVDD before power supply other than LVDD is turned ON/OFF. (*)

- Power ON: LVDD → (power supply other than LVDD)
- Power OFF: (power supply other than LVDD) → LVDD

* Reliability issues may arise if LVDD is cut off and a power supply other than LVDD is provided for 1 second or longer.

8. Electrical Characteristics

8.3 DC Characteristics

8.3.1 Current consumption

Item	Code	Condition	Min.	Typ.	Max.	Unit
Power supply current (*)						
Power supply current	IDDH0	UVDD3 = 3.6V	-	5 *2	-	mA
	IDDH1	CVDD = 5.5V	-	5 *3	-	mA
	IDDH2	VRIN = 5.5V	-	30 *4	-	mA
	IDDH3	VBUS_5V_IN = 5.5V	-	*5	-	mA
	IDDL	LVDD = 1.95V	-	25 *2	-	mA
Static current						
Power supply current	IDDS	Max. condition of each power supply Fixed to power supply or GND	-	-	TBD	μA
Input leak						
Input leakage current	IL	Max. condition of each power supply	-5	-	5	μA

*1: Based on the recommended operating conditions (Ta = -25°C)

*2: LSI operating current in our company's evaluation board environment (no use of built-in regulator, external power supply used)

*3: LSI operating current in our company's evaluation board environment

*4: LSI operating current in our company's evaluation board environment when using the built-in regulator

*5: Dependent on the VBUS current of the USB device connected to this LSI

8.3.2 Input characteristics

Item	Code	Condition	Min.	Typ.	Max.	Unit
Input characteristics		Pin: LVDD-system pin				
"H" level input voltage	VIH1	LVDD = 1.95V	1.27	-	-	V
"L" level input voltage	VIL1	LVDD = 1.65V	-	-	0.57	V
Input characteristics (Schmitt)		Pin: CVDD-system pin				
"H" level trigger voltage	VT1+	CVDD = 5.5V	2.50	-	3.95	V
"L" level trigger voltage	VT1-	CVDD = 4.5V	0.85	-	2.40	V
Hysteresis voltage	$\Delta V1$	CVDD = 4.5V	0.3	-	-	V
Schmitt input characteristics (USB: FS)		Pin: DP, DM				
"H" level trigger voltage	VTU+	UVDD3 = 3.6V	1.1	-	1.8	V
"L" level trigger voltage	VTU-	UVDD3 = 3.0V	1.0	-	1.5	V
Hysteresis voltage	ΔVU	UVDD3 = 3.0V	0.1	-	-	V
Input characteristics (USB: FS differential input)		Pin: DP, DM pair				
Differential input sensitivity	VDSU	UVDD3 = 3.0V Differential input voltage: 0.8 to 2.5 V	-	-	0.2	V
Input characteristics		Pin: Pull-up I/O pin				
Pull-up resistance	RPLU	VI = CVDD	50	-	150	k Ω
Input characteristics		Pin: Pull-down I/O pin (excluding TSTEN)				
Pull-down resistance	RPLD	VI = CVDD	50	-	150	k Ω
Input characteristics		Pin: TSTEN				
Pull-down resistance	RPLDL	VI = LVDD	100	-	200	k Ω
Input characteristics		Pin name: VBUS				
Pull-down resistance	RPLDB	VI = 5.0V	110	125	150	k Ω

8. Electrical Characteristics

8.3.3 Output characteristics

(V_{SS}=0V)

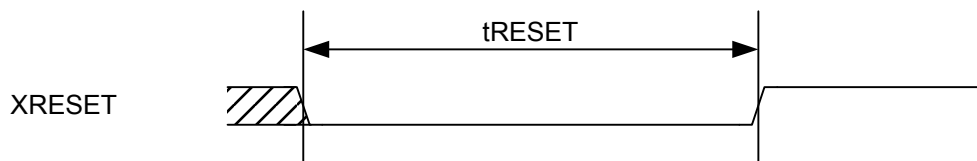
Item	Code	Condition	Min.	Typ.	Max.	Unit
Output characteristics	Pin:	CVDD-system pin				
“H” level output voltage	VOH1	CVDD = 4.5V IOH = -5.0mA	CVDD - 0.4	-	-	V
“L” level output voltage	VOL1	CVDD = 4.5V IOL = 5.0mA	-	-	0.4	V
Output characteristics (USB: FS)	Pin:	DP, DM				
“H” level output voltage	VOHUF	UVDD3 = 3.0V	2.8	-	-	V
“L” level output voltage	VOLUF	UVDD3 = 3.6V	-	-	0.3	V
Output characteristics	Pin:	CVDD-system pin				
OFF-STATE leakage current	IOZ	CVDD = 5.5V VOH = CVDD or SVDD VOL = VSS	-5	-	5	uA

8.3.4 Pin capacitance

Item	Code	Condition	Min.	Typ.	Max.	Unit
Pin capacitance	Pin name:	All input pins				
Input pin capacitance	CI	f = 1MHz	-	-	TBD	pF
Pin capacitance	Pin name:	All output pins				
Output pin capacitance	CO	f = 1MHz	-	-	TBD	pF
Pin capacitance	Pin name:	All output pins except DP and DM				
Input/output pin capacitance	CB	f = 1MHz	-	-	TBD	pF
Pin capacitance	Pin name:	DP, DM				
Input/output pin capacitance (USB)	CBU	f = 1MHz	-	-	TBD	pF

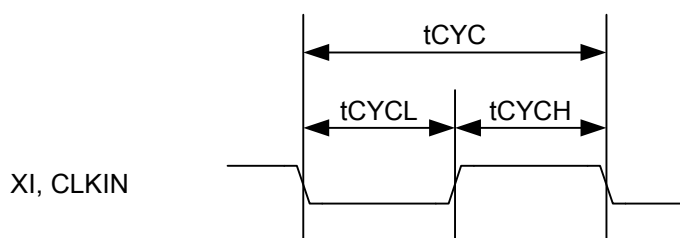
8.4 AC Characteristics

8.4.1 Reset timing



Code	Description	min	typ	max	Unit
tRESET	Reset pulse width	40	-	-	ns

8.4.2 Clock timing



Code	Description	Min.	Typ.	Max.	Unit
tCYC	Clock cycle (CLKSEL = "L")	-	12.000	-	MHz
tCYC	Clock cycle (CLKSEL = "H")	-	24.000	-	MHz
tCYCL tCYCH	Clock duty	45	50	55	%

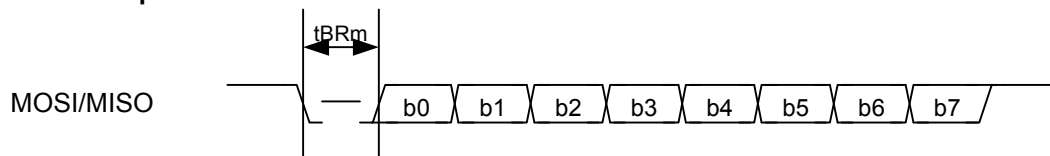
8.4.3 USB I/F timing

Complies with USB 2.0 (Universal Serial Bus Specification Revision 2.0) standard.

8. Electrical Characteristics

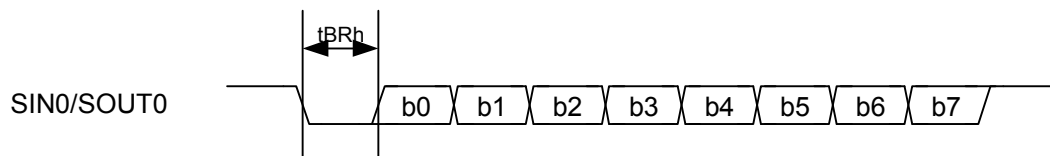
8.4.4 Serial I/F (main CPU) timing (SPI not supported by S1R72U01)

In UART operation



Code	Description	Min.	Typ.	Max.	Unit
tBRm	Baud rate	300	-	3M	bps

8.4.5 Serial I/F (history display) timing



Code	Description	Min.	Typ.	Max.	Unit
tBRh	Baud rate	-	38400	-	bps

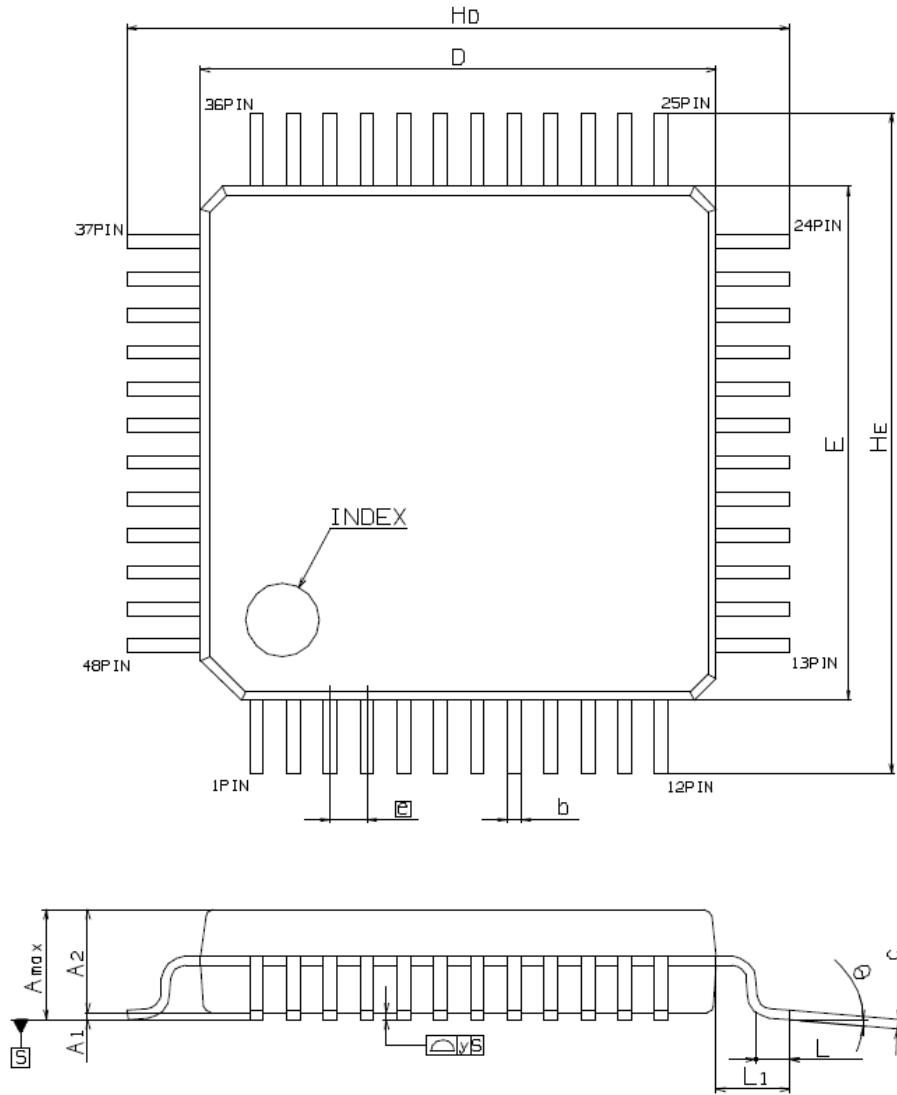
9. Connection Examples

Refer to the *S1R72U01 Evaluation Board Manual*.

10. External Dimensions Diagrams

10. External Dimensions Diagrams

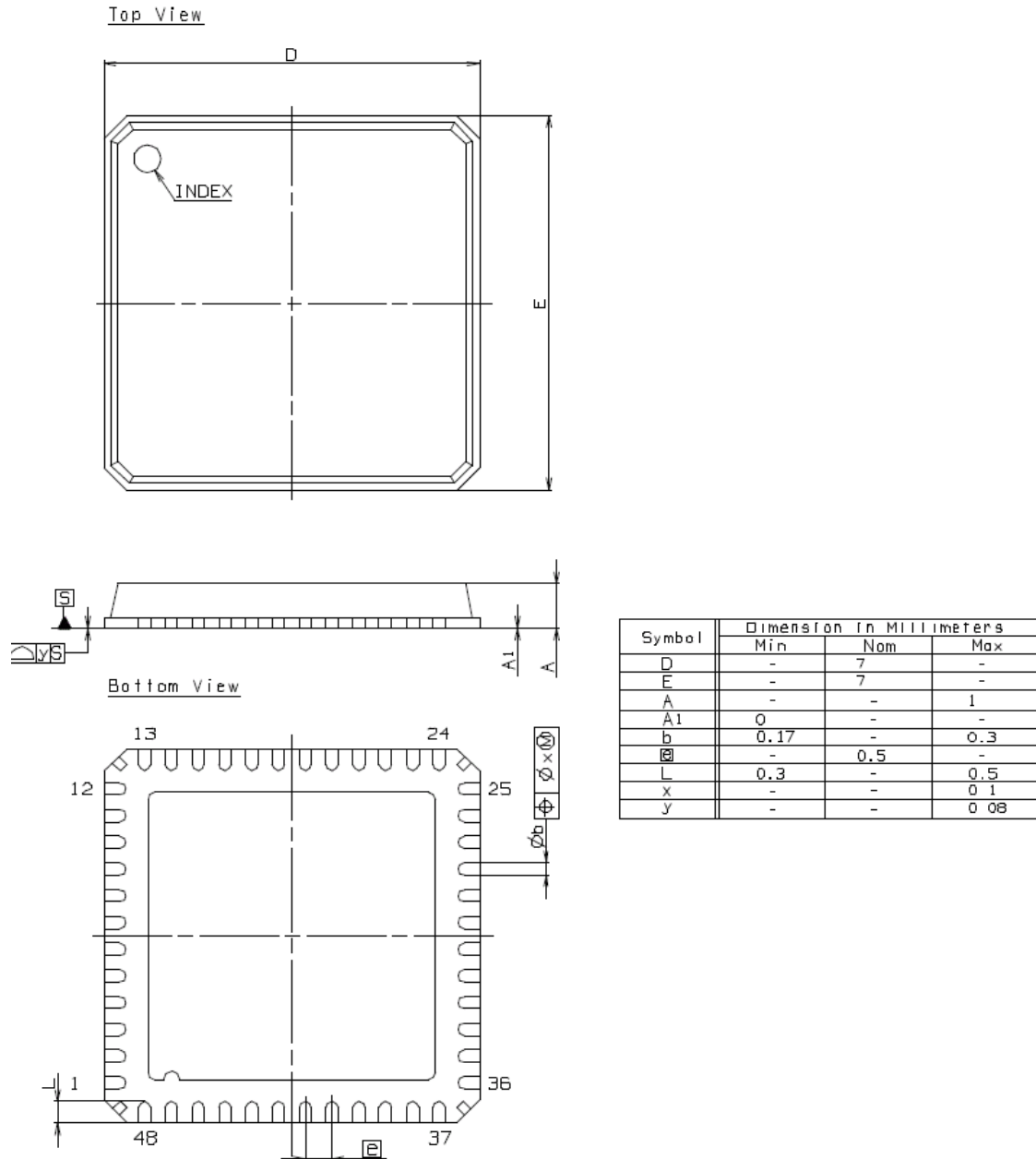
10.1 QFP12-48



Symbol	Dimension in Millimeters		
	Min	Nom	Max
E	-	7	-
D	-	7	-
A_{max}	-	-	1.7
$A1$	-	0.1	-
$A2$	-	1.4	-
\square	-	0.5	-
b	0.13	-	0.27
c	0.09	-	0.2
θ	0°	-	10°
L	0.3	-	0.7
$L1$	-	1	-
HE	-	9	-
Hb	-	9	-
y	-	-	0.08

1 = 1mm

10.2 QFN7-48



1 = 1mm

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